WHAT IS CLAIMED IS:

1. A TFT array substrate for use in a liquid crystal display device, the TFT array substrate comprising:

a gate line arranged in a transverse direction over a substrate;

a metallic oxide layer surrounding the gate line;

a data line arranged in a longitudinal direction perpendicular to the gate line over the substrate;

a thin film transistor formed near the crossing of the gate and data lines, the thin film transistor comprising:

a gate electrode over the substrate, the gate electrode being extended from the gate line and surrounded by the metallic oxide;

a gate insulation layer on the metallic oxide surrounding the gate electrode;

an active layer and an ohmic contact layer formed on the gate insulation layer;

a source electrode formed on the ohmic contact layer over the gate electrode and extended from the data line; and

a drain electrode formed on the ohmic contact layer over the gate electrode and spaced apart from the source electrode;

a protection layer formed over said thin film transistor, the protection layer having a drain contact hole that exposes a portion of the drain electrode; and

a pixel electrode formed in a pixel region that is defined by the gate and data lines, the pixel electrode contacting the drain electrode through the drain contact hole.

2. A TFT array substrate according to claim 1, wherein the metallic oxide is one of tantalum oxide (TaO_X), chrome oxide (CrO_X), titanium oxide (TiO_X) and tungsten oxide (WO_X).

3. A TFT array substrate according to claim 2, wherein the gate line and the gate electrode are copper (Cu).

4. A TFT array substrate according to claim 1, further comprising: a buffering layer between the substrate and the gate line and gate electrode.

5. A TFT array substrate according to claim 4, wherein the

metallic oxide is one of tantalum oxide (TaO_x) and titanium oxide (TiO_x) that are respectively made from tantalum (Ta) and titanium (Ti).

6. A TFT array substrate according to claim 4, wherein the buffering layer is one of tantalum nitride (TaN) and titanium nitride (TiN).

7. A TFT array substrate according to claim 4, wherein the buffering layer is one of silicon nitride (SiN_x) and silicon oxide (SiO_2).

8. A method of forming a TFT array substrate for use in a liquid crystal display device, comprising:

forming a first metal layer over a substrate;

forming a second metal layer on the first metal layer;

patterning the first and second metal layers so as to form a gate line and a gate electrode;

thermally-treating the substrate having the patterned first and second metal layers so as to diffuse material from the patterned first metal layer over the patterned second metal layer and then to form a

metallic oxide layer surrounding the second metal layer by oxidizing the diffused material of the first metal layer;

forming a gate insulation layer on the substrate, the gate line and the metallic oxide layer;

forming an amorphous silicon layer on the gate insulation layer;

forming an impurity-doped amorphous silicon layer on the amorphous silicon layer;

forming a third metal layer on the impurity-doped amorphous silicon layer;

patterning the third metal layer so as to form a data line, a source electrode and a drain electrode;

patterning the impurity-included amorphous silicon layer using the patterned third metal layer as masks so as to form an ohmic contact layer and a channel region in the amorphous silicon layer between the source and drain electrodes;

forming a protection layer on the amorphous silicon layer and on the patterned third metal layer;

patterning the protection layer, the amorphous silicon layer and the gate insulation layer except portions that correspond to the patterned third metal layer and channel region;

depositing a transparent conductive material in a pixel region that is defined by the gate and data lines; and

patterning the transparent conductive material so as to form a pixel electrode that contacts the drain electrode.

9. A method according to claim 8, wherein the first metal layer is one of tantalum (Ta), chrome (Cr), titanium (Ti) and tungsten (W).

10. A method according to claim 9, wherein the metallic oxide layer is one of tantalum oxide (TaO_X), chrome oxide (CrO_X), titanium oxide (TiO_X) and tungsten oxide (WO_X).

11. A method according to claim 8, wherein the second metal layer is copper (Cu).

12. A method according to claim 8, wherein the third metal layer is one of chrome (Cr), tantalum (Ta), titanium (Ti), tungsten (W) and molybdenum (Mo).

13. A method according to claim 8, further comprising: forming a buffering layer on the substrate before forming the first metal layer.

14. A method according to claim 13, wherein thermal treatment of the substrate is performed at a temperature of greater than 400°C.

15. A method according to claim 13, wherein the buffering layer is one of tantalum nitride (TaN) and titanium nitride (TiN).

16. A method according to claim 13, wherein the buffering layer is one of silicon nitride (SiN_X) and silicon oxide (SiO_2).

17. An insulated conductor structure for use in a TFT array substrate of a liquid crystal display device, the conductor structure comprising:

a substrate;

a metallic conductive line arranged over said substrate;

a metallic conductive electrode arranged over said substrate and branching off said conductive line;

a metallic oxide layer surrounding said gate line; and

an insulation layer on said conductive line and said metallic oxide layer.

18. The conductor structure according to claim 17, wherein said metallic oxide is one of tantalum oxide (TaO_X), chrome oxide (CrO_X), titanium oxide (TiO_X) and tungsten oxide (WO_X), respectively.

19. The conductor structure according to claim 18, further comprising a buffering layer between the substrate and each of said conductive line and said conductive electrode.

20. The conductor structure according to claim 19, wherein the buffering layer is one of tantalum nitride (TaN), titanium nitride (TiN), silicon nitride (SiN_X) and silicon oxide (SiO_2).

21. The conductor structure according to claim 17, wherein said conductive line is a gate line and said conductive electrode is a gate electrode.

22. The conductor structure of claim 17, wherein said conductive line and said conductive electrode are made of copper (Cu).

23. A method of forming an insulated conductor structure for use in a TFT array substrate of a liquid crystal display device, the method comprising:

providing a substrate;

forming a first metal layer over a substrate;

forming a second metal layer on the first metal layer;

patterning the first and second metal layers so as to form a conductive line and a conductive electrode thus defining an intermediate structure;

thermally treating said intermediate structure so as to diffuse material from the patterned first metal layer over the patterned second metal layer and then to form a metallic oxide layer surrounding the patterned second metal layer; and

forming an insulation layer on the substrate, the conductive line and said metallic oxide layer.

24. The method according to claim 23, wherein the first metal layer is one of tantalum (Ta), chrome (Cr), titanium (Ti) and tungsten (W) and the metallic oxide is one of tantalum oxide (TaO_x), chrome oxide (CrO_x), titanium oxide (TiO_x) and tungsten oxide (WO_x), respectively.

25. The method according to claim 23, wherein the second metal layer is copper (Cu).

26. A method according to claim 23, further comprising:

forming a buffering layer on the substrate before forming the first metal layer.

27. A method according to claim 26, wherein the buffering layer is one of tantalum nitride (TaN), titanium nitride (TiN), silicon nitride (SiN_x) and silicon oxide (SiO_2).